GUJARAT TECHNOLOGICAL UNIVERSITY

Bachelor of Engineering

Subject Code: 3171111
B. E. Semester: VII
Subject Name: Testing and Verification

Type of course: Introductory course for VLSI testing and verification

Rationale: This course provides a platform for students to understand importance of testing, fundamental VLSI test principles, basic concepts of design of testability (DFT), logic simulation and fault simulation, and verification concepts.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
				Theory Marks		Practical Marks		
L	T	P	C	ESE (E)	PA (M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Contents:

Sr No	Course Content	Teaching hours
1	**Introduction:** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.	**8**
2	**Design and Testability:** Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability	**14**
3	**Logic and Fault Simulation:** Introduction, Simulation Models, Logic Simulation, Fault Simulation	**10**
4	**Verification:** Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages	**5**
5	**Verification Techniques using System Verilog:** Linting, Simulation, Verification Intellectual Property, Waveform Viewers, Code Coverage, Functional Coverage, Verification Language Technologies, Assertions, Revision Control, Issue Tracking, Metrics	**8**
Total		**45**

Reference Books:

1. VLSI Test Principles and Architectures, Wang Wu Wen, Morgan Kaufmann Publishers
2. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", M. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2000
3. Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990
4. Introduction to Formal Hardware Verification, T.Kropf, Springer Verlag, 2000
5. System-on-a-Chip Verification- Methodology and Techniques, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001

6. Janick Bergeron, Writing Testbenches, Functional Verification of HDL Models, Springer
7. Janick Bergeron, Writing Testbenches using SystemVerilog, Springer

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
10	**15**	**15**	**15**	**15**	**0**

Legends: R: Remembrance; U = Understanding; A = Application and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table

Course Outcome:

1	To realize importance and challenges of VLSI Testing at different abstraction levels.	5 %
2	To study and apply various fault models for generation of test vectors.	15 %
3	To calculate observability and controllability parameters of given circuit and improve its testability and convert given circuit into scan design.	30 %
4	To apply concepts of logic simulation and fault simulation in designing and testing of VLSI circuits.	25 %
5	To identify the different characteristics of verification, and apply different verification methods.	10 %
6	To study different Verification techniques using System Verilog and improve different coverages.	15 %

Suggested List of Experiments:

1	Write a VHDL/Verilog code to realize functioning of Observation Point Insertion technique.
2	Write a VHDL/Verilog code to realize functioning of control Point Insertion technique.
3	Write VHDL/Verilog code for MUX-D scan cell and Level Sensitive/edge triggered muxed-D scan cell.
4	Write a VHDL/Verilog code to realize functioning of clocked scan cell and LSSD scan cell design.
5	Write a VHDL/Verilog code to realize functioning of LSSD double latch design
6	Write a VHDL/Verilog code to realize functioning of Mixing negative-edge and positive-edge scan cell in a scan chain
7	Write a VHDL/Verilog code to realize functioning of Fixing bus contention in scan design rules.
8	Write a VHDL/Verilog code to realize functioning of Adding a lock-up latch between cross-clock-domain scan cells.
9	To develop an exhaustive test bench for lower level combinational designs: 1. Adder and 2. multiplexer.
10	To develop an exhaustive test bench for J-K flip-flop.
11	To develop an exhaustive test bench for 4 bit up-down counter.

12	To verify an 8 bit shift register.
13	To prepare a complete test vector set for all possible stuck at faults parity checker where the data word is of 2 bit.
14	To develop an exhaustive SystemVerilog testbench to obtain different Types of Code Coverage Metrics for full adder design.
15	To develop an exhaustive SystemVerilog testbench to obtain functional coverage for full adder design.
16	To prepare an assertion based SystemVerilog testbench to verify 4x1 Multiplexer.
17	To obtain different types of Code Coverage Metrics for full adder design.
18	To obtain functional coverage for given design.
19	To perform assertion based verification for given design.

Suggested list of learning resources:

1. ngspice or any other simulation tool
2. www.nptel.ac.in
3. www.ocw.mit.edu
4. www.mosis.com
5. www.berkeley.edu